APPLICATION

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TITLE: SRAM CELL WITH WELL CONTACTS AND P+ DIFFUSION CROSSING TO GROUND OR N+ DIFFUSION CROSSING TO VDD

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SRAM CELL WITH WELL CONTACTS AND P+ DIFFUSION CROSSING TO GROUND OR N+ DIFFUSION CROSSING TO VDD

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to a low cost SRAM (Static Random Access Memory) cell with P and N well contacts and preferably with a P+ diffusion crossing to ground, and more particularly pertains to a low cost design for a SRAM cell that is complete at the M2 metal level and has improved cell passgate leakage, functionality and fabrication yields.

2. Discussion of the Prior Art

[0002] Initially, all dimensions shown in Figures 1, 2, 4 and 5 are in microns, and Figures 1 and 2 also show the dimensions in microns of the SRAM cell size.

[0003] Figure 1 illustrates a top plan view of a circuit lay-out of a prior art 90 nm node technology SRAM cell. Figure 1 illustrates only the PC (polysilicon conductor) areas, the RX (active silicon conductor regions which are isolated by trench isolation regions) regions, and the M1 (first metal) level of the SRAM cell and chip, and the M2 and M3 (second and third metal) levels are not shown.

[0004] Figure 2 illustrates a simplified version of Figure 1, and shows only the PC and RX areas and regions of the SRAM cell and chip, and the M1 metal level is not shown.

[0005] The prior art 90 nm node technology SRAM cell is fabricated in a base PC (Polysilicon Conductor) level, the overlying bottom M1 metal level, the next higher metal level M2, and the next higher metal layer M3. The prior art 90 nm node technology SRAM cell is fabricated with a PC level wordline WL having a crooked V shape at 10 and an M2 metal level bitline BL. For large SRAM arrays, the PC level is not an efficient enough conductor for the global wordlines, and the M3 metal level must be used for the global wordlines.

[0006] In summary, the PC level contains the wordlines WL, the M2 metal level contains the ground GND and the VDD power supply (which are connected through the M1 metal layer, shown in Figure 1 as M1 GND and M1 VDD, which connect to adjacent SRAM cells) and the bitlines BL, and the M3 metal level contains the global wordlines. The prior art SRAM cell includes 8.5 CA (contacts), 2 V1 (vias), and no PW (P Well) and NW (N Well) contacts which requires that additional real estate be provided on the chip outside the circuit shown in Figure 1 for periodic contacts to the PWs and NWs.

[0007] Figure 3 illustrates a circuit schematic of the prior art 90 nm node technology SRAM cell. The circuit of the prior art 90 nm node technology SRAM cell is well known and includes cross coupled pnp pull-up devices P1, P2 and npn pull-down devices N1, N2, with the P1, P2 devices being connected to the power supply VDD, and the N1, N2 devices being connected directly to ground GND. The left npn passgate NL is coupled between the left bitline BL and the junction of devices P1 and N1, with its gate coupled to the wordline WL. The right npn passgate NR is coupled between the right bitline BR and the junction of devices P2 and N2, with its gate coupled to the wordline WL

[0008] Referring to Figure 1 and more clearly to Figure 2, the PC (Polysilicon Conductor) level WL extends horizontally across the lower portion of the chip with a V shaped dip 10 in the middle, and crosses left and right legs of a bottom M shaped N+RX (active silicon conductor) region, with the crossing on the left defining the passgate NL, with the WL defining the gate G and the RX region defining the source S and drain D regions of the passgate NL, and with the

crossing on the right defining the passgate NR, with the WL defining the gate G and the RX region defining the source S and drain D regions of the passgate NR.

[0009] Left and right PC regions extend vertically on opposite left and right portions of the SRAM cell as shown in Figures 1 and 2.

[0010] The top horizontal portion of the bottom M shaped RX region crosses the left PC region and defines the pulldown device N1, with the left PC region defining the gate G and the RX region defining the drain D and source S regions of the pulldown device N1. The top horizontal portion of the M shaped RX region crosses the right PC region and defines the pulldown device N2, with the right PC region defining the gate G and the RX region defining the source S and drain D regions of the pulldown device N2, with a common source region S between the pulldown devices N1 and N2.

[0011] A horizontal base of a top W shaped P+RX (active silicon conductor) region crosses the upper portions of the left and right PC regions.

[0012] The bottom horizontal portion of the top W shaped RX region crosses the left PC region and defines the pullup device P1, with the left PC region defining the gate G and the RX region defining the drain D and source S regions of the pullup device P1. The bottom horizontal portion of the W shaped RX region crosses the right PC region and defines the pullup device P2, with the right PC region defining the gate G and the RX region defining the source S and drain D regions of the pullup device P2, with a common source region S between the pullup devices P1 and P2.

[0013] As illustrated in Figure 1, the V shape of the PC level word line WL snakes around the GND contact CA 12. The PC level word line WL snaking around the GND contact 12 is the main reason for the M3 metal level global word lines, and for a 45 degree PC level slant over the passgates as shown at 10.

[0014] The prior art cell behavior becomes erratic with RX/PC mask/level misalignments.

[0015] The passgate leakage of fabricated SRAM cells has also fluctuated from lot to lot and has been excessively high in most cases.

[0016] A demand exists for low cost SRAM cells, complete at the M2 metal level, and with better control over cell passgate leakage.

SUMMARY OF THE INVENTION

[0017] The present invention provides a low cost SRAM cell with well contacts and preferably a P+ diffusion crossing to ground or alternatively a N+ crossing to VDD, and more particularly provides a low cost design for a SRAM cell that is complete at the M2 metal level and has improved cell passgate leakage, functionality and fabrication yields.

[0018] The SRAM cell includes P well and N well contacts and preferably a P+ diffusion crossing to ground. The SRAM cell is complete at the M2 metal level and has improved cell passgate leakage, functionality and fabrication yields. The SRAM cell comprises cross coupled pnp pull-up devices P1, P2 and npn pull-down devices N1, N2, with the P1, P2 devices being connected to the power supply VDD, and the N1, N2 devices being coupled through a P+ diffusion region to ground. A first passgate is coupled between a first bitline and the junction of the devices P1 and N1, with its gate coupled to a wordline, and a second passgate is coupled between a second bitline and the junction of devices P2 and N2, with its gate coupled to the wordline.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The foregoing objects and advantages of the present invention for a SRAM cell with well contacts and P+ diffusion crossing to ground or N+ diffusion crossing to VDD may be more readily understood by one skilled in the art with reference being had to the following detailed description of several embodiments thereof, taken in conjunction with the

accompanying drawings wherein like elements are designated by identical reference numerals throughout the several views, and in which:

[0020] Figure 1 illustrates a top plan view of a circuit lay-out of a prior art 90 nm node technology SRAM cell and illustrates only the PC (polysilicon conductor) areas, the RX (active silicon conductor region isolated by trench isolation regions) regions, and the M1 level of the SRAM cell, and the M2 and M3 metal levels are not shown.

[0021] Figure 2 illustrates a simplified version of Figure 1, and shows only the PC and RX areas and regions of the SRAM cell, and the M1 metal level is not shown.

[0022] Figure 3 illustrates a circuit schematic of the prior art 90 nm node technology SRAM cell.

[0023] Figure 4 illustrates a top plan view of a circuit lay out of a preferred embodiment of a SRAM cell of the present invention, and illustrates only the PC areas, the RX regions, and the M1 level of the SRAM cell and chip, and the M2 and M3 metal levels are not shown.

[0024] Figure 5 illustrates a simplified version of Figure 4, and shows only the PC and RX areas and regions of the SRAM cell and chip, and the M1 metal level is not shown.

[0025] Figure 6 illustrates a circuit schematic of the SRAM cell of the present invention.

[0026] Figure 7 is a schematic diagram of an alternative embodiment of a PFET passgate cell which is similar in concept to the schematic diagram of Figure 6, but wherein all N devices are changed to P devices, all P devices are changed to N devices, and VDD and GND have been reversed.

DETAILED DESCRIPTION OF THE INVENTION

[0027] In the prior art SRAM cell, the PC level word line WL snaking at 10 around the GND contact 12 is the main reason for M3 metal level global word lines, and for the 45 degree PC level slant over the passgates. Moreover, a pseudo anchor 14 of the pulldown NFETs at the PC level is needed to minimize shorting at 16 between the PC level corner and the CA level corner, and because of the pseudo anchor, the PC level word line WL has to be notched down at the edge of the passgate at 18.

[0028] In recognition of these problems in the prior art, the present invention shifts the GND contact 40 to the boundary of the cell as shown in Figure 4. The GND contact for the pulldown NFETs is then connected through a P+ diffusion crossing 42 formed between the P Well and the center leg of a bottom M shaped RX region, as illustrated in Figure 5.

[0029] The present invention provides low cost SRAM cells, complete at the M2 metal level, having improved cell passgate leakage, functionality and fabrication yields, with P and N well contacts and a P+ diffusion crossing to ground.

[0030] Figure 4 illustrates a top plan view of a circuit lay out of a preferred embodiment of a SRAM cell of the present invention, and illustrates only the PC (polysilicon conductor) areas, the RX (active silicon conductor region isolated within trench isolation regions) regions, and the M1 level of the SRAM cell, and the M2 and M3 metal levels are not shown.

[0031] Figure 5 illustrates a simplified version of Figure 4, and shows only the PC and RX areas and regions of the SRAM cell, and the M1 metal level is not shown.

[0032] Figure 4 illustrates a top plan view of the lay out of a SRAM cell pursuant to the present invention. The SRAM cell of the present invention has a straight PC level word line WL because of the repositioned GND contact 40, and an M2 metal level bitline BL. The M1 metal level is now used for the global wordlines GWL, as shown by M1 GWL, and also for the power supply VDD, as shown by M1 VDD. In summary, the PC level contains the wordlines WL, the

M1 metal level contains the global wordlines GWL and the VDD power supply, and the M2 metal level contains the bitlines BL and the ground GND, and the M3 metal level is not used in the construction of the SRAM cell.

[0033] The SRAM cell of the present invention includes 8.0 CA (contacts), less than the 8.5 CA (a 0.5 CA is caused by sharing of a CA) of the prior art, 1.5 V1 (vias), less than the 2.0 V1 of the prior art, and also provides PW and NW contacts.

[0034] Figure 6 illustrates a circuit schematic of the SRAM cell of the present invention. Similar to the circuit of the prior art SRAM cell, the circuit includes cross coupled pnp pull-up devices P1, P2, and npn pull-down devices N1, N2, with the P1, P2 devices being connected to the power supply VDD. The N1, N2 devices are coupled through the P+ diffusion region, shown as a 0.5K resistor to ground GND, which is different from the prior art SRAM cell. The left npn passgate NL is coupled between the left bitline BL and the junction of devices P1 and N1, with its gate coupled to the wordline WL. The right npn passgate NR is coupled between the right bitline BR and the junction of devices P2 and N2, with its gate coupled to the wordline WL.

[0035] Referring to Figure 4 and more clearly to Figure 5, the PC WL extends horizontally straight across the lower portion of the SRAM cell (without a V shaped dip 10 in the middle as in the prior art), and crosses left and right legs of a bottom M shaped N+RX region, with the crossing on the left defining the passgate NL, with the WL defining the gate G and the RX region defining the source S and drain D regions of the passgate WL, and with the crossing on the right defining the passgate NR with the WL defining the gate G and the RX region defining the source S and drain D regions of the passgate WR.

[0036] Left and right PC regions extend vertically on opposite left and right portions of the SRAM cell as shown in Figures 4 and 5.

[0037] The top horizontal portion of the bottom M shaped RX region crosses the left PC region and defines the pulldown device N1, with the left PC region defining the gate G and the RX region defining the drain D and source S regions of the pulldown device N1. The top horizontal portion of the M shaped RX region crosses the right PC region and defines the pulldown device N2, with the right PC region defining the gate G and the RX region defining the source S and drain D regions of the pulldown device N2, with a common source region S between the pulldown devices N1 and N2.

[0038] A horizontal base of a top W shaped P+RX region crosses the upper portions of the left and right PC regions.

[0039] The bottom horizontal portion of the top W shaped RX region crosses the left PC region and defines the pullup device P1, with the left PC region defining the gate G and the RX region defining the drain D and source S regions of the pullup device P1. The bottom horizontal portion of the W shaped RX region crosses the right PC region and defines the pullup device P2, with the right PC region defining the gate G and the RX region defining the source S and drain D regions of the pullup device P2, with a common source region S between the pullup devices P1 and P2.

[0040] Figure 4 illustrates the position of the PW contact in the lower portion of the cell, and also illustrates the position of the NW contact added around the VDD supply in the upper portion of the cell. Figures 4 and 5 illustrate the position of a lower dotted mask BP1 which is used to form a P+ diffusion into the active silicon of the RX region. The P Well contact, shown as PW CONT, is formed in the overlap area/region of the center leg of the bottom M shaped RX region over the P+ diffusion within the area of the dotted mask BP1. Figures 4 and 5 also illustrate the position of an upper dotted mask BP2 which is used to form an N+ diffusion into the active silicon of the RX region, and the N Well contact, shown as NW CONT, is formed in the overlap area/region of the center leg of the upper W shaped RX region over the N+ diffusion within the area of the dotted mask BP2.

[0041] The overall benefits of the present invention are as follows:

Invention	Prior Art	Benefits
straight local PC local WL	crooked PC local WL	no overlay concerns no uncontrollable leakages or malfunctions
horizontal M1 for global word line	no free M1 channel	low cost design doesn't need M3 no concern of PC word line drop
M1 VDD, M2 GND & BL	M2 VDD & GND, M2 BL	more sturdy GND bus
8 CA, 1.5 V1	8.5 CA, 2V1	better yield
built-in well contacts	well contacts outside cell	smaller array layout less well leakage, smaller chance of latchup

[0042] The cost of these benefits is the extra resistance of the P+ diffusion to GND contact, which is about 500 ohms for this particular layout, and is formed at the intersection of the PC word line and the P+ diffusion runner reaching to the GND contact.

[0043] It is like a PFET over PW instead of over NW.

[0044] Read access from WL switching up to BL difference of 200 mv degrades by ~5% to 0.6 ns from 0.57 ns, which is negligible for 90 nm node technology circuit designs which have a typical cycle time ranging from 2 ns to 10 ns. Moreover, any degradation in read access is compensated for by a similar amount of improvement in write time.

[0045] Noise margins are tabulated below. Again, there is slight degradation, but the delta would be less than the accuracy of simulations.

	half-select Invention	half-select Prior Art	standby Invention	standby Prior Art
Inm0 (ua)	41.1	41.2	79.7	84.3
Inm1 (ua)	11.0	11.5	27.8	27.9
Vnm0 (mv)	339	351	447	439
Vnm1 (mv)	624	634	754	761

[0046] This ground resistance can be eliminated with a P+ channel implant at the crossing of the P+ diffusion and the PC.

[0047] A similar concept can be implemented in an alternative embodiment of a PFET passgate cell, in which case, the crossing would be with N+ diffusion to VDD. Figure 7 is a schematic diagram of a PFET passgate cell which is similar in concept to the schematic diagram of Figure 6, but wherein all N devices are changed to P devices, all P devices are changed to N devices, and VDD and GND have been reversed.

[0048] While several embodiments and variations of the present invention for an SRAM cell with well contacts and P+ diffusion crossing to ground or N+ diffusion crossing to VDD are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.